REMARKS

In the November 8, 2007 Office Action, the Examiner:

- Rejected claims 6, 13, 21, 38-46 and 50-52 under 35 U.S.C. § 112, second paragraph, as being indefinite;
- Rejected claims 1, 2, 4-6, 8-11, 13-17, 19-21, 23-25, 27, 29, 31-39, 41, 42, 44-47, 49, 50, and 52 under 35 U.S.C. § 102(a) as being anticipated by the SFF-8053 Specification for GBIC (Gigabit Interface Converter) Rev. 5.5, September 27, 2000 ("SFF Committee"); and
- Rejected claims 3, 18, 26, and 40 under 35 U.S.C. § 103(a) as unpatentable over SFF Committee in view of Keevill et al. ("Keevill," U.S. Pat. No. 6,359,938 B1).
- Rejected claims 7, 22, 30, and 43 under 35 U.S.C. § 103(a) as unpatentable over SFF Committee in view of Baltz et al. ("Baltz," U.S. Pat. No. 6,469,906 B1).
- Rejected claims 12 and 28 under 35 U.S.C. § 103(a) as unpatentable over SFF Committee in view of Levinson (U.S. Pat. No. 5,019,769 A).
- Rejected claims 48 and 51 under 35 U.S.C. § 103(a) as unpatentable over SFF Committee.

After entry of this amendment, the pending claims remain claims 1-52.

Amendments to the Claims

Claims 6, 13, 21, and 38 include limitations directed to the SFF and GBIC standards. These claims inherently encompass the standards as in effect at the time of filing the present application. Any reasonable interpretation of these limitations could not expect them to cover a standard not yet envisioned or in effect at the time of filing. Despite the definiteness of these claims, Applicants have amended the above-mentioned claims to limit them to the SFF and GBIC standards in effect as of the filing date of the present application.

Claim 3 has been amended to correct a typographical error.

Claim 53 is new. Support for the claimed analog-to-digital conversion circuitry and comparison logic is found, for example, in Figure 2 of the specification. The claim

limitations regarding the analog-to-digital conversion circuitry and comparison logic mirror claim language allowed by the Examiner in Application No. 09/777,917, which has issued as U.S. 7,079,775. The present application claims priority to Application No. 09/777,917, which is incorporated by reference in its entirety. Accordingly, claim 53 is patentable over the prior art.

No new matter has been added.

Claim Rejections - 35 U.S.C. § 112

The Examiner has rejected claims 6, 13, 21, 38-46, and 50-52 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the Examiner states that the claims are indefinite because they refer to industry standards that may vary in scope over time. Claims 39-46 and 50-52 were rejected because they depend on claim 38. Applicants have amended the claims to limit them to the SFF and GBIC standards in effect as of the filing date of the present application. In light of these amendments, Applicants respectfully submit that these indefiniteness rejections are now moot.

Claim Rejections - 35 U.S.C. § 102

The Examiner has rejected claims 1, 2, 4-6, 8-11, 13-17, 19-21, 23-25, 27, 29, 31-39, 41, 42, 44-47, 49, 50, and 52 under 35 U.S.C. § 102(a) as being anticipated by the SFF-8053 Specification for GBIC (Gigabit Interface Converter) Rev. 5.5 ("SFF Committee"). For a proper showing that SFF Committee anticipates these claims, SFF Committee must disclose all elements of each rejected claim. The rejected claims contain three independent claims, namely claims 1, 17, and 38.

Independent claims 1 and 38 specify that a "controller IC" includes "a serial digital interface configured to facilitate communication, between the optoelectronic module and a host, of ***diagnostic parameter information*** concerning the optoelectronic component" (emphasis added). Independent claim 17 specifies that "a controller IC" includes "a serial digital interface configured and arranged to facilitate communication, between the optical transceiver module and a host, of ***diagnostic parameter information***" (emphasis added). Each independent claim further specifies that the "serial digital interface" is in communication with "a pair of pins" included in "a pinout arrangement." Therefore, the

claimed "pair of pins" is in communication with the "controller IC," since the "serial digital interface" is included in the "controller IC."

The Examiner states that the claimed "controller IC" is disclosed by the "Laser Drive Safety Control" in Figure 1 of SFF Committee, as shown below:

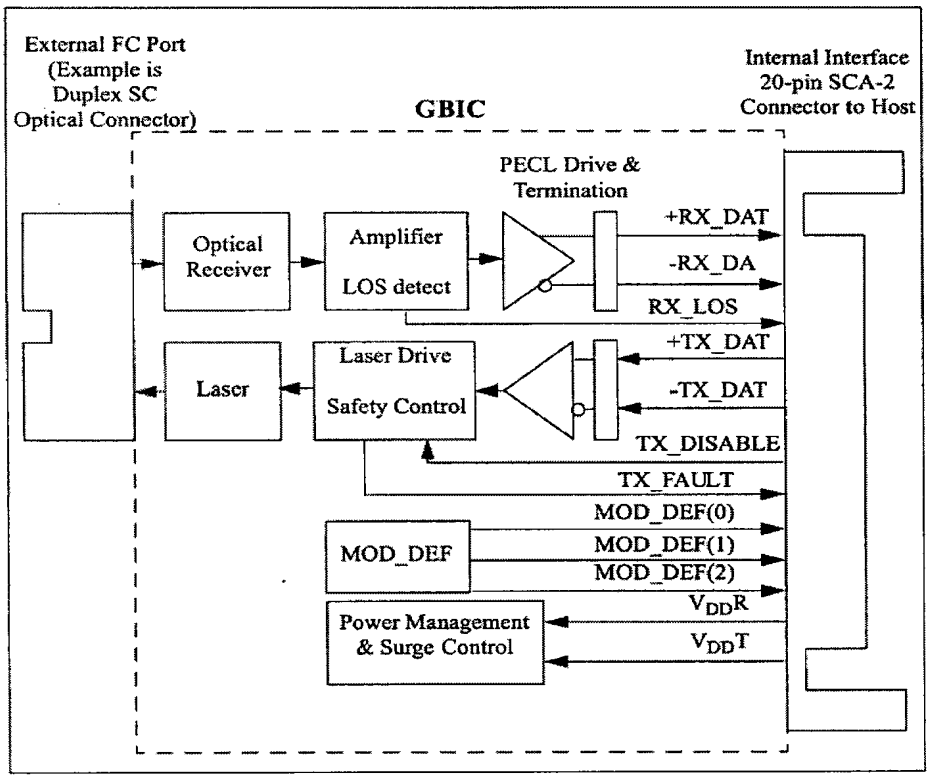

Figure 1: Functional diagram of typical shortwave laser GBIC

The Examiner also argues that the claimed "pair of pins" in communication with the "serial digital interface" of the "controller IC" is disclosed by "serial clock signal 'SCL' on pin 5 and serial data signal 'SDA' on pin 6." Office Action of 12/08/07, at 4. The use of pins 5 and 6 for SCL and SDA signals, as well as for the MOD_DEF(1) and MOD_DEF(2) signals shown in Figure 1, is described in Table 8 of SFF Committee. Note that in Figure 1 shown above, the MOD_DEF(1) and MOD_DEF(2) signal lines are also used for I2C communications, through pins 5 and 6. *See* SFF Committee at 12. The MOD_DEF signals provide module definition information stored in the "MOD_DEF" block of Figure 1 and the SCL and SDA signals provide information stored in an EEPROM. *See id.* at 11-13.

Pins 5 and 6, however, are not in communication with a "serial digital interface" that is part of a "controller IC" and that is configured to "facilitate communication . . . of diagnostic parameter information," as the independent claims require. Instead, pins 5 and 6 only communicate with the "MOD_DEF" block and with the EEPROM. *See id.* fig. 1 and

tbl. 8, at 4, 12 (describing communication with the "MOD_DEF" block); *id.* at 12-13 and app. D, at 43-52 (describing communication with the EEPROM). Neither the "MOD_DEF" block nor the EEPROM communicates "diagnostic parameter information": the MOD_DEF block merely provides "module definition" information and the EEPROM merely provides "sophisticated identification information." *See id.* at 11-12 (MOD_DEF block); 43-52 (EEPROM). Furthermore, neither the "MOD_DEF" block nor the EEPROM can be characterized as a "controller IC." The function of these two elements is limited to storing and providing information and does not include controlling other elements in the transceiver. *See id.*

Because SFF Committee does not describe a "a pair of pins" in communication with the "serial digital interface" of a "controller IC" that facilitates communication of "diagnostic parameter information," SFF Committee does not disclose, teach, or suggest all of the limitations of each independent claim. In light of the above, it is respectfully submitted that SFF Committee cannot anticipate independent claims 1, 17, and 38, or any of the claims that depend there from, as the reference fails to teach at least two limitations of each of these claims.

Claim Rejections - 35 U.S.C. § 103

The Examiner has rejected claims 3, 18, 26, and 40 under 35 U.S.C. § 103(a) as unpatentable over SFF Committee in view of Keevill. Regarding claims 3, 18, and 40, the Examiner argues that SFF Committee discloses every limitation except the serial digital interface being compatible with I^2C or MDIO serial communication, which Keevill discloses. Regarding claim 26, the Examiner argues that SFF Committee discloses every limitation except that "at least one of the plurality of memory mapped locations is implemented as a register," which Keevill discloses.

The Examiner has rejected claims 7, 22, 30, and 43 under 35 U.S.C. § 103(a) as unpatentable over SFF Committee in view of Baltz. The Examiner argues that SFF Committee discloses every limitation except the particular pin arrangements specified in these claims, which Baltz discloses.

The Examiner has rejected claims 12 and 28 under 35 U.S.C. § 103(a) as unpatentable over SFF Committee in view of Levinson. Regarding claim 12, the Examiner argues that SFF Committee discloses every limitation except an analog monitoring connection, which Levinson discloses. Regarding claim 28, the Examiner argues that SFF Committee discloses

every limitation except that "at least one of the memory mapped locations is configured to receive and store information concerning at least one of" the specified group of "diagnostic parameters."

The Examiner has rejected claims 48 and 51 under 35 U.S.C. § 103(a) as unpatentable over SFF Committee. The Examiner argues that the claimed pin arrangement is merely a design choice.

The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of skill in the art. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966); *see also KSR Int'l Co. V. Teleflex Inc.*, 127 S.Ct. 1727, 1734 (2007). "Section 103 forbids issuance of a patent when the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR*, 127 S.CT. at 1734 (internal quotations omitted). Thus, to be patentable, the differences between the claimed subject matter and the prior art must be substantial enough to not be obvious to a person of ordinary skill in the art.

In considering the scope of the prior art and the differences between the prior art and the present claims, the Examiner relies on SFF Committee as disclosing every limitation of the independent claims on which the rejected claims depend. As discussed above regarding the § 102 rejections, however, SFF Committee does not describe a "controller IC" that includes "a serial digital interface" that facilitates communication of "diagnostic parameter information" and that is in communication with a "pair of pins." The features described by these limitations represent a substantial difference between the prior art and the present claims; their absence from earlier transceiver limited their functionality, as explained in the Background and Summary of the present invention. *See* ¶¶ [0006]-[0017]. Accordingly, because these substantial features are absent from the prior art, the present claims are not obvious in view of the prior art.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the application is now in a condition for allowance. However, should the Examiner believe that the claims are not in condition for allowance, the Applicant encourages the Examiner to call the undersigned attorney at 650-843-7519 to set up an interview.

Respectfully submitted,

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